Subject Code: 01CE0402

Subject Name: Computer Organization and Architecture

B.Tech. Year - II

Objective: To conceptualize the concepts of organizational and architectural issues of a digital computer. Further, analyse performance issues in processor and memory design of a digital computer. Also, understanding various data transfer techniques in digital computer and to analyse processor performance improvement using instruction level parallelism.

Credits Earned: 4 Credits

Course Outcomes: After completion of this course, student will be able to

- Understand and describe the basics of various architectural units of the Computer System
- Apply the knowledge of combinational and sequential logical circuits to mimic a simple computer architecture
- Recognize the importance of parallelism in computer architecture.
- Ability to understand the concept of cache mapping techniques.
- To eliminate or remove stall by altering order of instructions.

Pre-requisite of course: Fundamentals of Computer, Digital Logic Circuits.

Teaching and Examination Scheme

Teaching Scheme (Hours)			Credits	Theory Marks			Tutorial/ Practical Marks		Total Marks
Theory	Tutorial	Practical		ESE (E)	Mid Sem (M)	Internal (I)	Viva (V)	Term work (TW)	
3	2	0	4	50	30	20	25	25	150

Contents:

Unit	Topics	Contact Hours
1	**Computer Data Representation & Register Transfer and Micro-operations:** Basic computer data types, Complements, Fixed point representation, Floating point representation, Register Transfer language, Register Transfer, Bus and Memory Transfers (Three-State Bus Buffers, Memory Transfer), Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro-Operations, Arithmetic logical shift unit	8
2	**Introduction to Computer Organization and Design:** Instruction codes, Computer registers, Computer instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-output and interrupt, Complete computer description.	6
3	**Fundamental concepts of Micro programmed Control:** Control Memory, Address sequencing, Micro program Example, design of control Unit	4
4	**Concepts of Central Processing Unit:** Introduction, General Register Organization, Stack Organization, Instruction format, Addressing Modes, data transfer and manipulation, Program Control, Reduced Instruction Set Computer (RISC)	8
5	**Introduction to Pipeline:** Flynn's taxonomy, Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction, Pipeline, RISC Pipeline,	4
6	**Basic of Computer Arithmetic:** Introduction, Addition and subtraction, Multiplication Algorithms (Booth Multiplication Algorithm), Division Algorithms, Floating Point Arithmetic operations, Decimal Arithmetic Unit.	6
7	**Input-Output Organization:** Input-Output Interface, Asynchronous Data Transfer, Modes Of Transfer, Priority Interrupt, DMA, Input-Output Processor (IOP), CPUIOP Communication, Serial communication.	4
8	**Memory Classification and Organization:** Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory.	4
	Total Hours	**44**

References:

1. M. Morris Mano, Computer System Architecture, Pearson

2. Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization, Sixth Edition, PHI

3. M. Murdocca & V. Heuring, Computer Architecture & Organization, WILEY

4. John Hayes, Computer Architecture and Organization, McGrawHill

Suggested Theory distribution:

The suggested theory distribution as per Bloom's taxonomy is as per follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery and evaluation					
Remember	Understand	Apply	Analyze	Evaluate	Create
20%	20%	30%	15%	10%	5%

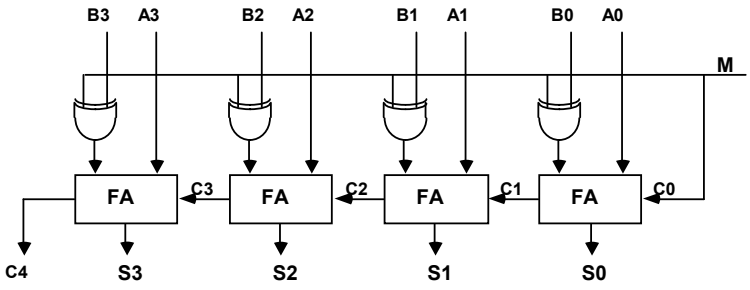
Suggested List of Tutorials:

1. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. **(Applying)**
   a. How many selection inputs are there in each multiplexer ?
   b. What size of multiplexers are needed?
   c. How many multiplexers are there in the bus ?
2. The following transfer statements specify a memory. Explain the memory operation in each case. **(Comprehension)**

   R2 ←M[AR]
   M[AR]←R3
   R5←M[R5]

3. The adder-subtractor circuit in following Fig has the following values for input mode M and data inputs A and B. In each case, determine the values of the outputs : S3, S2, S1, S0 and C4. **(Comprehension)**

	M	A	B
I.	0	0111	0110
II.	0	1000	1001
III.	1	1100	1000
IV.	1	0101	1010
V.	1	0000	0001



4. Design a 4-bit combinational circuit decrementer using four full-adder circuits. **(Synthesis)**

5. Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive-NOR, NOR, and NAND. Use two selection variables. Show the logic diagram of one typical stage. **(Synthesis)**

6. Register **A** holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value in A to :
   I. 01101101
   II. 11111101 **(Comprehension)**

7. The 8bit registers AR, BR, CR and DR initially have the following values :
   AR = 11110010 BR = 11111111
   CR = 10111001 DR = 11101010

Determine the 8bit values in each register after the execution of the following sequence of micro-operations.

AR ←AR + BR
CR ←CR Λ DR, BR ← BR + 1
AR ← AR – CR **(Comprehension)**

8. An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (whileIEN = 1).
   I. What instruction must be placed at address 1 ?
   II. What must be the last two instruction of the output program? **(Comprehension)**
9. Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory? **(Comprehension)**
10. Define the following: (a) microoperation; (b) microinstruction; (c) microprogram; (d) microcode. **(Knowedge)**
11. Explain how the mapping from an instruction code to a microinstruction address can be done by means of a read-only memory. What is the advantage of this method? **(Comprehension)**
12. Show how a 9-bit microoperation field in a microinstruction can be divided into subfields to specify 46 microoperations. How many microoperations can be specified in one microinstruction? **(Application)**

13. A computer has 16 registers, an ALU (Arithmetic Logic Unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.

a. Formulate a control word for a microoperation.

b. Specify the number of bits in each field of the control word and give a general encoding scheme.

c. Show the bits of the control word that specify the microoperation: R4→R5+R6. **(Application, Synthesis)**

14. Convert the following arithmetic expressions from infix to reverse Polish notation. **(Comprehension)**

a. **A * B + C * D + E * F**

b. **A * B + A * (B * D + C * E)**

c. **A + B * [C * D + E * (F + G)]**

d. $$\frac{A * [B + C * (D + E)]}{F * (G + H)}$$

15. Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment. **(Synthesis)**

16. Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching. **(Comprehension)**

17. Perform the arithmetic operations below with binary numbers and with negative numbers in signed-2's complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position. **(Application)**

(a) (+35) + (+40) (b) (– 35) + (– 40) (c) (–35) – (+40)

18. Prove that the multiplication of two n-digit numbers in base r gives a product no more than 2n digits in length. Show that this statement implies that no overflow can occur in the multiplication operations. **(Application)**

19. Design an array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders. **(Synthesis)**

20. Show the hardware to be used for the addition and subtraction of two decimal numbers with negative numbers in signed-10's complement representation. Indicate how an overflow is detected. Derive the flowchart algorithm and try a few numbers to convince yourself that the algorithm produces correct results. **(Application)**

Instructional Method:

a. The course delivery method will depend upon the requirement of content and need of students. The teacher in addition to conventional teaching method by black board, may also use any of tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

b. The internal evaluation will be done on the basis of continuous evaluation of students in the laboratory and class-room.

c. Students will use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory

Supplementary Resources:

1. NPTEL Lecture Series
2. http://www.intel.com/pressroom/kits/quickreffam.htm
3. web.stanford.edu/class/ee282/