Syllabus of Diploma Engineering

Computer Engineering

Semester: - IV

Subject Name: Computer Organization

Subject Code: 09CE0401

Objective: To conceptualize the basics of organizational and architectural issues of a digital computer. Further, analyse performance issues in processor and memory design of a digital computer. Also, understanding various data transfer techniques in digital computer and to analyse processor performance improvement using instruction level parallelism.

Credits Earned: 3 Credits

Course Outcomes: After completion of this course, student will be able to

- Understand and describe the basics of various architectural units of the Computer System
- Apply the knowledge of combinational and sequential logical circuits to mimic a simple computer architecture
- Recognize the importance of parallelism in computer architecture.
- Ability to understand the concept of cache mapping techniques.
- To eliminate or remove stall by altering order of instructions.

Pre-requisite of course: Fundamentals of Computer, Digital Logic Circuits.

Teaching and Examination Scheme

Teaching Scheme (Hours)			Credits	Theory Marks			Tutorial/ Practical Marks		Total Marks
Theory	Tutorial	Practical		ESE (E)	Mid Sem (M)	Internal (I)	Viva (V)	Term work (TW)	
3	0	0	3	50	30	20	0	0	100

Contents:

Unit	Topics	Contact Hours
1	**Computer Data Representation & Register Transfer and Micro-operations:** Basic computer data types, Number representation, Complements, Register Transfer language, Register Transfer, Bus and Memory Transfers (Tree-State Bus Buffers, Memory Transfer), Arithmetic Micro-Operations, Logic Micro-Operations, Shift Micro-Operations, Arithmetic logical shift unit	8
2	**Basic Computer Organization and Design:** Instruction codes, Computer registers, Computer instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-output and interrupt, Complete computer description.	8
3	**Programming Basic Computer:** Introduction, Machine Language, Assembly Language, Assembler, Program Loops, Arithmetic and Logic operations, subroutines	6
4	**Central Processing Unit and Pipeline Processing:** Introduction, General Register Organization, Stack Organization, Instruction format, Addressing Modes, data transfer and manipulation, Program Control, Reduced Instruction Set Computer (RISC), CISC, parallel processing	8
5	**Input-Output Organization:** Input-Output Interface, Asynchronous Data Transfer, Modes Of Transfer, Priority Interrupt, DMA, Input-Output Processor (IOP), CPUIOP Communication, Serial communication.	6
6	**Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory.	6
	Total Hours	**42**

References:

1. M. Morris Mano, Computer System Architecture, Pearson

2. Andrew S. Tanenbaum and Todd Austin, Structured Computer Organization, Sixth Edition, PHI

3. M. Murdocca & V. Heuring, Computer Architecture & Organization, WILEY

4. John Hayes, Computer Architecture and Organization, McGrawHill

Suggested Theory distribution:

The suggested theory distribution as per Bloom's taxonomy is as per follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery and evaluation					
Remember	Understand	Apply	Analyze	Evaluate	Create
35%	35%	30%	0%	0%	0%

Instructional Method:

a. The course delivery method will depend upon the requirement of content and need of students. The teacher in addition to conventional teaching method by black board, may also use any of tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

b. The internal evaluation will be done on the basis of continuous evaluation of students in the class-room.

c. Students will use supplementary resources such as online videos, NPTEL videos, e-courses.

Supplementary Resources:

1. NPTEL Lecture Series
2. http://www.intel.com/pressroom/kits/quickreffam.htm
3. web.stanford.edu/class/ee282/