INSTITUTE	**FACULTY OF ENGINEERING AND TECHNOLOGY**
PROGRAM	**BACHELOR OF TECHNOLOGY (COMPUTER SCIENCE AND ENGINEERING -CYBER SECURITY)**
SEMESTER	**2**
COURSE TITLE	**DIGITAL ELECTRONICS**
COURSE CODE	**01EC0102**
COURSE CREDITS	**4**

Objective:

1 To understand the basic of Digital Electronic concepts required in the analysis and design of digital electronic circuits and systems.
To understand the number system, logic gates, Boolean algebra, etc. To understand Construction and operation of various digital circuits such as Adder, Subtractor, Multiplexer, Demultiplexer, Decoder, Encoder, Flip-flops, Counters, Registers and memory devices. To devolve the capability to Simplify, Analyze and Design the Various Digital Electronic Circuits.

2 To understand the basic of Digital Electronic concepts required in analysis and design of digital electronic circuits and systems. To understand the number system, logic gates, Boolean algebra, etc. To understand Construction and operation of various digital circuits such as Adder, Subtractor, Multiplexer, Demultiplexer, Decoder, Encoder, Flip-flops, Counters, Registers and memory devices. To devolve the capability to Simplify, Analyze and Design the Various Digital Electronic Circuits.

3 To understand the basic of Digital Electronic concepts required in analysis and design of digital electronic circuits and systems.
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4 • To understand the basic of Digital Electronic concepts required in analysis and design of digital
electronic circuits and systems.

5 • To understand the number system, logic gates, Boolean algebra, etc.

6 • To understand Construction and operation of various digital circuits such as Adder, Subtractor,

7 • Multiplexer, Demultiplexer, Decoder, Encoder, Flip-flops, Counters, Registers and memory
devices.

8 • To devolve the capability to Simplify, Analyze and Design the Various Digital Electronic Circuits.

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Objective:

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10 The subject aims to prepare the students,
To understand the basic of Digital Electronic concepts required in analysis and design of digital
electronic circuits and systems.
To understand the number system, logic gates, Boolean algebra, etc.
To understand Construction and operation of various digital circuits such as Adder, Subtractor,
Multiplexer, Demultiplexer, Decoder, Encoder, Flip-flops, Counters, Registers and memory devices.
To devolve the capability to Simplify, Analyze and Design the Various Digital Electronic Circuits.

Course Outcomes: After completion of this course, student will be able to:

1 Develop understanding of basic digital circuits like logic gates, logic families, flip flops and memory devices

2 Use knowledge of various number systems and binary codes to solve conversion problems.

3 Apply concepts of Boolean algebra and other minimization techniques for digital circuit design.

4 Design digital circuits using different combinational and sequential logic.

5 Implement various combinational and sequential circuits using appropriate hardware/simulation.

Pre-requisite of course: To understand the basic of Digital Electronic concepts required in analysis and design of digital electronic circuits and systems.

Teaching and Examination Scheme

Theory Hours	Tutorial Hours	Practical Hours	ESE	IA	CSE	Viva	Term Work
3	0	2	50	30	20	25	25

Contents : Unit	Topics	Contact Hours
1	**Orientation Day - Introduction of Digital Electronics** Introduction	

Contents : Unit	Topics	Contact Hours
2	**Module-1** Introduction of subject, Analogue versus Digital, Various number system (base 2,8,10 & 16), Various Number Systems and Conversion between them, Various Binary Codes and its application	
3	**Module-2** Logic gates truth table Verification using ICs & MultiSim, De Morgan's Theorem & NAND and NOR Universal gate, NAND and NOR Universal gate practice & Miscellaneous practices, Basic Rules of Binary Addition and Subtraction, Binary Multiplication and Division, Binary Addition and Subtraction using Complements	
4	**Module -3** Positive & Negative logic, IEEE/ANSI Symbols, Floating Point & Accuracy of conversion, Opportunity Session, 555 Timer concept & Its modes	
5	**Module- 4** Logic families Characteristics parameters & Classification, TTL, ECL Families, Introduction of Quartus	
6	**Module-5** Boolean Algebra & Simplification Technique, Boolean Equation Simplification using K-map, 5 Variable K-map & Miscellaneous Practice, Project Literature Survey presentation	
7	**Module-6** Adder, Subtractor, Multiplexer and Demultiplexer, Encoder Decoder, Comparator, parity generator circuits, Code converter circuits	
8	**Module 7** Basic Flip Flops, Counter Design, State Machine Design	
9	**Number Systems and Codes** Session-1 To understand the number systems, Session 2 Next numbers, Session-3 Number systems conversion	
10	**Digital Arithmetic** Session-8 To implement binary arithmetic rules to simplify the boolean equations, Session-9 To understand basic rules of complements in any number system. 2. To perform the subtraction using 1's complement, 2's complement., Session-10 To perform the subtraction using 7's, 8's, 9's, 10's complement & 15's, 16's Complement methods.	
11	**Logic Gates and Related Devices** Session-4 logic gates design, ICs and Its truth table., Session-5 Practice and Hands on logic gates design, Session-6 De-Morgan's Theorem and Universal gate, Session-7 To implement the logic circuits and Boolean equations using logic gates	

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Contents : Unit	Topics	Contact Hours
12	**Logic Families** Session-11 To understand various logic families and parameters, Session-12 To understand Logic Families Characteristics Parameters & Classification of Logic Families, Session-13 To understand various logic families & comparison of different logic families	
13	**Boolean Algebra and Simplification Techniques** Session-14 Boolean algebra and simplification techniques, Session-15 Boolean reduction techniques to minimize circuits, Session-16 K-map for 2,3,4 variable, Session-17 K-MAP simplification for SOP and POS representation, Miscellaneous Assignment, Kmap Practice assignment-1, Kmap Practice assignment-2, To understand K-MAP simplification for 5 variables, 5 variables K-Map Assignment	
14	**Combinational Logic Circuits** To design and verify the Half adder, Full adder., To design and verify Half subtractor, full subtractor and four-bit adder circuit., To design and verify the Multiplexer and Demultiplexer circuits., To design and verify the Encoder and Decoder circuits., Multiplexer, Demultiplexer, Encoder, Decoder Circuits assignment, To design and verify the comparator, parity generator circuits., Quartus implementation of various circuits-1, Quartus implementation of various circuits-2, Code convertor circuits., Code convertor circuits implementation.	
15	**Sequential Logic Circuits** To understand the Flip Flop., Flip Flop design and its truth table., Ripple Counter, Synchronous Counter, Various types of counters, Designing Counter with Arbitrary Sequences, Shift Register, Shift Register Counters, IEEE/ANSI Symbols for counters and Registers, To design Counter for various applications.	
16	**Memory Devices** Introduction of Computer system and memory	
17	**Hardware Project** Hardware Project Session-1, Hardware Project Session-2, Hardware Project Session-3, Hardware Project Session-4	
18	**Long Hour Design** LHD on Quartus	
19	**Number System and Codes** Analog Vs Digital, Number System, Number system conversion, Accuracy of conversion , Floating point Numbers, Binary codes	5
20	**Logic Gates and related devices** Positive/Negative logic, Logig GATES, symbol, truthtable , Gate implemtation in simulator , Universal GATE , Gates with Open Collector/Drain output, Tristate Gates, AND-OR-INVERT Gates,, Schmitt Gates, Special Output Gates, Fan-Out of Logic Gates, Buffers and Transceivers	5

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Contents : Unit	Topics	Contact Hours
21	**Digital Arithmetic** Basic Rules of Binary Addition and Subtraction, Binary Addition and Subtraction using Complements, BCD Addition and Subtraction, Binary Multiplication and Division, Floating-Point Arithmetic	4
22	**Logic Families** Significance of Families, Characteristic Parameters, Types of Logic Families: TTL, ECL, CMOS, Bi-CMOS, NMOS and PMOS, Comparison between various logic families. Interfacing between CMOS and TTL logic families	3
23	**Boolean Algebra and Simplification Techniques** Introduction, Postulates and Theorems, Various types of Boolean expressions, Simplification Techniques - Karnaugh Map Method and Tabulation Method	4
24	**Combinational Logic Circuits** Combinational Circuits and its implementations, Arithmetic Circuits - Adders and Subtractors, BCD Adder, Look-Ahead Carry Generator, ALU, Multiplier, Magnitude comparator, Multiplexer, Encoders, Demultiplexers and Decoders, Parity Generation and Checking	8
25	**Sequential Logic Circuits** R-S and D Flip-flop, Level Triggered and Edge-Triggered Flip-flops, J-K and T Flip-flop, Synchronous and Asynchronous Input, Flip-flop Timing Parameters, Application of Flip-flop, Ripple Counter, Synchronous Counter, Modulus Counter, Binary Ripple Counter, Synchronous Counters, UP/Down Counters, Decade and BCD Counters, Presettable Counters, Decoding Counter, Cascading Counter, Designing Counter with Arbitrary Sequences, Shift Register, Shift Register Counters, IEEE/ANSI Symbols for counters and Registers	10
26	**Memory Devices** Anatomy of Computer, A computer Systems, Anatomy of Computer, A computer Systems, Expanding Memory Capacity	3
Total Hours		**42**

Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
1	**Experiment - 1** Verify the truth tables of various Digital Logic Gates.	2
2	**Experiment - 2** Verify the application of NAND and NOR logic gates as universal gates.	2
3	**Experiment - 3** Implementation of Boolean Logic Functions using logic gate ICs.	2

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Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
4	**Experiment - 4** Implement the half-full adder, half-full subtractor using logic gates and verification of its operation.	2
5	**Experiment - 5** Perform and verify the Decoder and Encoder.	2
6	**Experiment - 6** Perform and verify various code converters a) Binary to Gray code b) BCD to Excess-3 code.	2
7	**Experiment - 7** Perform and verify 4x1 multiplexer and 1x4 de-multiplexer.	2
8	**Experiment - 8** Perform and verify the operation of RS latch, SR and D flip-flops.	2
9	**Experiment - 9** Perform and verify the operation of JK and T flip-flops .	2
10	**Experiment - 10** Perform and verify the operation of shift registers.	2
11	**Experiment - 11** Perform and verify the operation of synchronous and asynchronous counter.	2
12	**Experiment - 12** Perform an experiment which demonstrates function of 4 bit or 8 bit ALU.	2
13	**Experiment - 13** Design mono-stable multi-vibrator using 555 timer.	2
14	**Experiment - 14** Design bi-stable multi-vibrator using 555 timer.	2
15	**Experiment - 15** Design astable multivibrator using 555 timer	2
Total Hours		**30**

Textbook :

1 Modern Digital Electronics, R.P.Jain, WileyIndia, 2010

References:

1 Digital Electronics: Principles, Devices and Applications, Digital Electronics: Principles, Devices and Applications, Anil K. Maini, WileyIndia Pvt. Ltd, 2008

2 Digital Logic & State Machine Design", Digital Logic & State Machine Design", David J. Comer, Saunders College Pub., 1990

Suggested Theory Distribution:

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery and evaluation					
Remember / Knowledge	**Understand**	**Apply**	**Analyze**	**Evaluate**	**Higher order Thinking / Creative**
15.00	20.00	30.00	20.00	10.00	5.00

Instructional Method:

1. The course delivery method will depend upon the requirement of content and need of the students. The teacher in addition to conventional teaching method (Chalk and Talk) may use any of the tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc. for effective teaching
2. The internal evaluation will be done on the basis of continuous evaluation of students in the laboratory and class-room.
3. Practical examination will be conducted at the end of the semester for evaluation of performance of students in laboratory
4. Students may use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory, etc

Supplementary Resources:

1. https://www.coursera.org/learn/digital-systems
2. https://nptel.ac.in/courses/117105080/3
3. https://www.udemy.com/master-the-concepts-of-digital-circuit-design
4. https://electronicsforu.com/category/electronics-projects/hardware-diy
5. https://www.coursera.org/lecture/intro-fpga-design-embedded-systems/4-introducing-quartus-prime-0QeZn

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