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| COURSE TITLE | DIGITAL CMOS DESIGN |
| COURSE CODE | 01EC0307 |
| COURSE CREDITS | 4 |

Objective:

- 1 The course aims to develop a strong understanding of CMOS device operation and inverter characteristics, enabling students to analyse and design combinational and sequential circuits at transistor level. It focuses on evaluating delay, power, and noise in CMOS circuits while introducing layout design and physical design constraints. The course also provides hands-on exposure to modern EDA tools for practical implementation and verification.

Course Outcomes: After completion of this course, student will be able to:

- 1 Explain CMOS technology, fabrication processes, MOSFET operation, and non-ideal effects.
- 2 Design a CMOS inverter for given specifications and analyse the designed inverter with respect to key performance parameters.
- 3 Design and compare combinational and sequential logic circuits using various CMOS logic styles.
- 4 Critically comment on interconnect effects, scaling challenges, and perform CMOS layout design with verification techniques.

Pre-requisite of course: Basic understanding of semiconductor devices (PN junction, MOSFET operation), Fundamental knowledge of digital electronics (logic gates, Boolean algebra, combinational and sequential circuits)

Teaching and Examination Scheme

| Theory Hours | Tutorial Hours | Practical Hours | ESE | IA | CSE | Viva | Term Work |
|---------------------|-----------------------|------------------------|------------|-----------|------------|-------------|------------------|
| 3 | 0 | 2 | 50 | 30 | 20 | 25 | 25 |

| Contents : Unit | Topics | Contact Hours |
|------------------------|---|----------------------|
| 1 | CMOS Technology Fundamentals Evolution of MOS Technology and CMOS Scaling Trends, CMOS Fabrication Techniques (n-well, p-well, Twin-tub Processes), Structure and Operation of NMOS and PMOS Transistors, Current–Voltage Characteristics and MOS Capacitances, Threshold Voltage, Body Effect, and Device Parameters, Short-Channel Effects (Velocity Saturation and DIBL) | 6 |

| Contents : Unit | Topics | Contact Hours |
|----------------------------|--|--------------------------|
| 2 | CMOS Inverter Design & Analysis Structure and Operation of CMOS Inverter, Voltage Transfer Characteristics (VTC) of CMOS Inverter, Noise Margins and Noise Immunity (NMH and NML), Switching Threshold and Transistor Sizing, Static Behavior of CMOS Inverter, Dynamic Behavior of CMOS Inverter, Power Dissipation in CMOS (Static, Dynamic, Short-Circuit), Propagation Delay and Timing Analysis | 8 |
| 3 | Combinational Circuit Design using CMOS Static CMOS Logic Design Principles, Ratioed Logic Design, Pass Transistor Logic (PTL), Transmission Gate Logic, Design of Basic CMOS Gates (NAND, NOR, XOR), Implementation of Complex CMOS Logic Gates, Logical Effort and Gate Optimization, Fan-in and Fan-out Effects in CMOS Circuits | 8 |
| 4 | Sequential Circuit Design using CMOS Behavior of Bistable Elements and Memory Concepts, Design of SR Latch and D Latch, Master–Slave Flip-Flop Design, Transmission Gate Based Flip-Flop, Timing Parameters (Setup Time, Hold Time, Propagation Delay), Clocking Strategies in Sequential Circuits, Introduction to Dynamic Logic and Precharge–Evaluate Circuits, Domino Logic and Its Operation | 8 |
| 5 | Interconnects and Scaling Effects Interconnect Effects in VLSI Design, RC Delay Models and Elmore Delay Estimation, Analysis of Interconnect Parasitics, Technology Scaling and Associated Challenges, Power–Delay Trade-offs in VLSI Circuits, Low-Power Design Techniques | 6 |
| 6 | CMOS Layout Design and Verification Layout Design Rules and Lambda-Based Design Methodology, Stick Diagrams and Layout Representation Techniques, Layout of CMOS Inverter, Layout of CMOS Logic Gates, Parasitic Extraction in VLSI Layout, Design Rule Checking (DRC) and Layout Versus Schematic (LVS) Verification | 6 |
| Total Hours | | 42 |

Suggested List of Experiments:

| Contents : Unit | Topics | Contact Hours |
|----------------------------|---|--------------------------|
| 1 | Experiment No. 1 To study I–V characteristics of NMOS and PMOS transistors. | 2 |
| 2 | Experiment No. 2 To design CMOS inverter and analyse its characteristics (E.g. VTC, noise margins, switching threshold, propagation delay, power dissipation, etc.) | 2 |
| 3 | Experiment No. 3 To analyse the effect of transistor sizing on switching threshold for given design. | 2 |

Suggested List of Experiments:

| Contents : Unit | Topics | Contact Hours |
|--------------------|---|------------------|
| 4 | Experiment No. 4 To design and simulate CMOS NAND and NOR gates for given design specifications. | 2 |
| 5 | Experiment No. 5 To design XOR gate using CMOS logic for given design specifications and verify its operation. | 2 |
| 6 | Experiment No. 6 To implement logic function using CMOS design techniques. | 2 |
| 7 | Experiment No. 7 To design given digital circuit using pass transistor logic. | 2 |
| 8 | Experiment No. 8 To design given digital circuit using transmission gate logic. | 2 |
| 9 | Experiment No. 9 To analyse propagation delay using logical effort in combinational circuits. | 2 |
| 10 | Experiment No. 10 To design and simulate SR latch and D latch. | 2 |
| 11 | Experiment No. 11 To design and implement master-slave D flip-flop. | 2 |
| 12 | Experiment No. 12 To measure setup time and hold time in sequential circuits. | 2 |
| 13 | Experiment No. 13 To design and simulate transmission gate flip-flop. | 2 |
| 14 | Experiment No. 14 To implement dynamic logic circuits such as domino logic. | 2 |
| 15 | Experiment No. 15 To design CMOS layout of inverter and other logic gates and perform DRC and LVS verification. | 2 |
| Total Hours | | 30 |

Textbook :

- 1 CMOS Digital Integrated Circuits: Analysis and Design, Sung-Mo Kang, Yusuf Leblebici, McGraw-Hill Education, 2003
- 2 CMOS VLSI Design: A Circuits and Systems Perspective, Neil H. E. Weste, David Harris, Pearson Education, 2011

References:

- 1 Digital Integrated Circuits: A Design Perspective, Digital Integrated Circuits: A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Pearson Education, 2003
- 2 Handbook of Digital CMOS Technology, Circuits, and Systems, Handbook of Digital CMOS Technology, Circuits, and Systems, Karim Abbas, Springer, 2020

Suggested Theory Distribution:

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

| Distribution of Theory for course delivery | | | | | |
|--|------------|-------|---------|----------|----------------------------------|
| Remember / Knowledge | Understand | Apply | Analyze | Evaluate | Higher order Thinking / Creative |
| 5.00 | 10.00 | 30.00 | 20.00 | 20.00 | 15.00 |

Instructional Method:

- 1 The internal evaluation will be done based on the continuous evaluation of students in the laboratory and class-room.
- 2 A practical examination will be conducted at the end of the semester for evaluation of practical performance.
- 3 Students may use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory, etc.
- 4 The course delivery method will depend upon the requirements of content and need of the students. The teacher in addition to conventional teaching methods (Chalk and Talk) may use any of the tools/techniques such as demonstration, role play, Quiz, brainstorming, Flipped class, Project based learning, Collaborative learning, MOOCs etc. for effective teaching.

Supplementary Resources:

- 1 <https://nptel.ac.in/courses/117106092>
- 2 <https://ocw.mit.edu/courses/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/>
- 3 <https://www.coursera.org/learn/vlsi-cad>
- 4 <https://www.allaboutcircuits.com/textbook/digital/>
- 5 <https://www.electronics-tutorials.ws/>
- 6 <https://www.asic-world.com/>
- 7 <https://www.vlsiuniverse.com/>
- 8 <https://www.vlsigyan.com/>
- 9 <https://chipxpert.in/10-must-try-open-source-tools-for-every-vlsi-student-in-2025/>
- 10 https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM