COURSE TITLE	**DIGITAL DESIGN USING HDL**
COURSE CODE	**01EC0312**
COURSE CREDITS	**4**

Objective:

1 The course aims to familiarize students with Hardware Description Languages (HDL) for digital system design, enabling them to model combinational and sequential circuits. It focuses on understanding RTL design and synthesis concepts while promoting modular and optimized design approaches. It also introduces verification methods using test-benches to ensure accurate and reliable designs.

Course Outcomes: After completion of this course, student will be able to:

1 Implement HDL concepts and constructs to model and design digital systems using appropriate design practices and abstraction levels

2 Develop sequential logic designs using HDL by applying clocking techniques, timing considerations, and modular design approaches.

3 Assess performance of digital systems design using HDL with FSMs and modular modeling techniques.

4 Synthesize and verify digital systems to ensure correct and reliable functionality.

Pre-requisite of course: Basic understanding of digital electronics, Fundamental knowledge of electronic circuits and switching concepts

Teaching and Examination Scheme

Theory Hours	Tutorial Hours	Practical Hours	ESE	IA	CSE	Viva	Term Work
3	0	2	50	30	20	25	25

Contents : Unit	Topics	Contact Hours
1	**Introduction to Digital Design using HDL** Concept of Hardware Description Language (HDL), Need for HDL in Modern Digital System Design, Comparison of HDLs with Programming Languages, Overview of Verilog and VHDL with Industry Relevance, Digital Design Flow from Specification to Verification, Levels of Abstraction (Behavioral, RTL, Structural), Basic HDL Elements and Data Representation (Signals/Variables, Constants, Parameters/Generics, Bit-Widths, Multi-Valued Logic)	7
2	**HDL Constructs** Concurrent and Sequential Statements, Assignment Mechanisms (Continuous/Procedural or Signal/Variable Assignment), Use of Logical, Arithmetic, Relational, and Shift Operators, Conditional Constructs (if, case, Conditional Assignments), Loop Constructs for Iterative Design, Process / Always Blocks, Sensitivity Lists, Guidelines for Writing Synthesizable HDL Code	8

Contents : Unit	Topics	Contact Hours
3	**Sequential Logic Design in HDL** Modelling of Latches and Flip-Flops, Synchronous Design Concepts, Asynchronous Design Concepts, Clocking Strategies and Timing Considerations, Assignment Behavior (Blocking vs Non-Blocking / Signal vs Variable), Modular Design using Functions, Tasks / Procedures in HDL, Parameterized / Generic Design Techniques	8
4	**Digital System Modelling and Design** Modelling of Combinational Systems, Modelling of Sequential Systems, Finite State Machine Design (Moore and Mealy Models), State Encoding Techniques, Modelling of Multiplexers, Decoders, and Comparators, Modelling of Counters and Shift Registers, Modelling of ALU and Basic Datapath Elements	7
5	**HDL-Based Design Optimization** Efficient and Synthesizable HDL Coding Concepts, Resource Sharing and Optimization Techniques, Hierarchical Design for Code Reuse and Structuring, Timing and Area Considerations, Reduction of Redundant Logic, Performance Improvement Techniques	6
6	**Verification and Synthesis Concepts** Testbench Development (Stimulus Generation and Response Observation), Simulation and Debugging Techniques, Event Control and Timing Concepts (Delays and Clocking), Synthesis Concepts and Constraints, Avoidance of Unintended Latches and Race Conditions, Design Verification Methodologies	6
Total Hours		**42**

Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
1	**Experiment No. 1** To understand the basic structure of an HDL program including module definition, data types, constants, and parameters.	2
2	**Experiment No. 2** To implement basic logic gates using continuous assignment in HDL.	2
3	**Experiment No. 3** To design and simulate combinational circuits using dataflow modelling style.	2
4	**Experiment No. 4** To model combinational circuits using behavioral constructs such as if and case statements.	2
5	**Experiment No. 5** To study and analyze the difference between blocking and non-blocking assignments.	2

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Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
6	**Experiment No. 6** To implement arithmetic, logical, and relational operations using HDL constructs.	2
7	**Experiment No. 7** To design and simulate encoder and decoder circuits using behavioral modelling.	2
8	**Experiment No. 8** To design comparator and multiplexer circuits using case statements.	2
9	**Experiment No. 9** To model latch circuits using behavioral HDL constructs.	2
10	**Experiment No. 10** To design and simulate D flip-flops with synchronous and asynchronous reset.	2
11	**Experiment No. 11** To design and analyze different types of counters such as binary and modulo-N counters.	2
12	**Experiment No. 12** To implement and simulate shift registers including universal shift registers.	2
13	**Experiment No. 13** To design and simulate Moore and Mealy finite state machines.	2
14	**Experiment No. 14** To design a parameterized arithmetic logic unit (ALU) using modular HDL techniques.	2
15	**Experiment No. 15** To model and simulate memory elements such as register files or simple RAM.	2
16	**Experiment No. 16** To develop modular designs using tasks and functions in HDL.	2
17	**Experiment No. 17** To implement scalable designs using generate statements and parameterized modules.	2
18	**Experiment No. 18** To optimize HDL code by reducing redundancy and improving design efficiency.	2
19	**Experiment No. 19** To develop testbenches for verification of combinational and sequential circuits.	2
20	**Experiment No. 20** To verify HDL designs using delays and event control mechanisms in testbenches.	2

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Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
21	**Capstone Project** Students shall undertake the implementation of moderately complex digital system design projects, such as vending machines, elevator controllers, and traffic light controllers, applying the concepts and methodologies learned throughout the course.	0
Total Hours		**40**

Textbook :

1 A Verilog HDL Primer, J. Bhasker, Star Galaxy Publishing, 2018

2 Verilog HDL: A Guide to Digital Design and Synthesis, Samir Palnitkar, Prentice Hall, 2003

References:

1 Digital Design with an Introduction to Verilog HDL, VHDL, and System Verilog, Digital Design with an Introduction to Verilog HDL, VHDL, and System Verilog, M. Morris Mano and Michael D. Ciletti, Pearson Education, 2018

2 Advanced Digital Design with the Verilog HDL, Advanced Digital Design with the Verilog HDL, Michael D. Ciletti, Pearson Education, 2011

3 Circuit Design with VHDL, Circuit Design with VHDL, Volnei Pedroni, Prentice Hall of India (PHI), 2007

Suggested Theory Distribution:

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery					
Remember / Knowledge	**Understand**	**Apply**	**Analyze**	**Evaluate**	**Higher order Thinking / Creative**
5.00	10.00	30.00	20.00	20.00	15.00

Instructional Method:

1 The internal evaluation will be done based on the continuous evaluation of students in the laboratory and class-room.

2 A practical examination will be conducted at the end of the semester for evaluation of practical performance.

3 Students may use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory, etc.

4 The course delivery method will depend upon the requirements of content and need of the students. The teacher in addition to conventional teaching methods (Chalk and Talk) may use any of the tools/techniques such as demonstration, role play, Quiz, brainstorming, flipped class, Project based learning, Collaborative learning, MOOCs etc. for effective teaching.

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Supplementary Resources:

1. https://www.unrepo.com/verilog/what-is-verilog-a-detailed-tutorial
2. https://www.asic-world.com/verilog/veritut.html
3. https://acg.cis.upenn.edu/milom/cis371-Spring13/lab/textbook-verilog-tutorial/VOL/main.htm
4. https://fpgatutorial.com/verilog/
5. https://www.chipverify.com/verilog/verilog-tutorial
6. http://gmvhdl.com/VHDL.html
7. https://www.vhdl-online.de/
8. https://nptel.ac.in/courses/106105165
9. https://nptel.ac.in/courses/106105041
10. https://nptel.ac.in/courses/117105080
11. https://www.edaplayground.com/