COURSE TITLE	**DIGITAL VLSI TESTING**
COURSE CODE	**01CT0629**
COURSE CREDITS	**4**

Objective:

1 The objective of this course is to expose the students to the recent and fundamental VLSI test principles and DFT architectures. This will help them to design reliable and better quality products.

Course Outcomes: After completion of this course, student will be able to:

1 Apply the test patterns to verify the design
2 Analyze the various types of faults
3 Analyze the DFT architectures
4 Design fault simulation models

Pre-requisite of course: Digital Logic Design

Teaching and Examination Scheme

Theory Hours	Tutorial Hours	Practical Hours	ESE	IA	CSE	Viva	Term Work
3	0	2	50	30	20	25	25

Contents : Unit	Topics	Contact Hours
1	**Introduction** Importance, Challenges, Levels of abstraction, Fault Models, Advanced issues	8
2	**Design for Testability** Introduction, Testability Analysis, DFT Basics, , Scan cell design, Scan Architecture, Scan design rules, Scan design flow. , Fault Simulation: Introduction, , Simulation models, Logic simulation, Fault simulation	8
3	**Test Generation** Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms, ATPG for non stuck-at faults, Other issues in test generation , Built-In-Self-Test: Introduction, BIST design rules, , Built-In-Self-Test: Test pattern generation, Output response analysis, Logic BIST architectures	8
4	**Test Compression** Introduction, Stimulus compression, Response compression	6
5	**Memory Testing** Introduction, RAM fault models, RAM test generation, Memory BIST	6

MR. CHANDRASINH DHIRUBHA PARMAR
Digitally signed by (Name of HOD)

DR. RAJENDRASINH BAHADURSINH JADEJA
Digitally signed by (Name of Dean/ Principal)

Contents : Unit	Topics	Contact Hours
6	**Power and Thermal Aware Test** Importance, Power models, Low power ATPG, Powerand Thermal Aware Test: Low power BIST, Thermal aware techniques	6
Total Hours		**42**

Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
1	**Expeirments** Using a hardware description language (HDL) such as Verilog or VHDL to design basic gates. Simulate their functionality using test bench files., Implement and simulate stuck-at faults (SA0 and SA1) in combinational circuits. Evaluate fault coverage for a given test vector set., Generate test patterns using tools like Cadence or Mentor Graphics for a given combinational circuit. Verify fault coverage using simulation., Implement boundary scan architecture using IEEE 1149.1 standard for testing shift registers or small circuits., Design a BIST architecture for a simple combinational or sequential circuit. Validate fault detection through simulation, Add scan chains to a sequential circuit to enable testing. Verify functionality and fault coverage using a simulation tool., Analyze and test delay faults in sequential circuits using transition delay fault models., Design and test an arithmetic circuit such as a 4-bit ALU for stuck-at and delay faults. Validate fault coverage., Perform March tests (March C-, March X, etc.) on SRAM or DRAM models. Simulate test patterns for read, write, and stuck-at faults., Design an LFSR-based PRPG. Use it to generate test patterns for a small circuit and evaluate fault detection efficiency, Analyze the power consumption of test patterns in a combinational circuit. Optimize test patterns to reduce power usage during testing., Implement a diagnostic algorithm for multiple stuck-at faults in a digital circuit. Simulate the algorithm and evaluate fault diagnosis accuracy, Apply compression techniques (e.g., XOR networks) to reduce test data volume. Simulate and validate the efficiency of test compression, Insert DFT features like scan chains and BIST into a digital circuit using CAD tools. Evaluate the impact on test coverage and area overhead	28
Total Hours		**28**

Textbook :

1 Digital Systems and Testable Design, M. Abramovici, M.A. Breuer and A.D. Friedman, Jaico Publishing House. , 2017

2 Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, M.L. Bushnell and V.D. Agrawal, Kluwer Academic Publishers, 1997

References:

1 Digital Circuit Testing and Testability, Digital Circuit Testing and Testability, P.K. Lala, Academic Press, 2002

Suggested Theory Distribution:

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery					
Remember / Knowledge	**Understand**	**Apply**	**Analyze**	**Evaluate**	**Higher order Thinking / Creative**
0.00	20.00	30.00	30.00	10.00	10.00

Instructional Method:

1 The course delivery method will depend upon the requirement of content and need of students. The teacher in addition to conventional teaching method by black board, may also use any of tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc.

2 The internal evaluation will be done on the basis of continuous evaluation of students in the laboratory and class-room.

3 Practical examination will be conducted at the end of semester for evaluation of performance of students in laboratory

4 Students will use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory.

Supplementary Resources:

1 https://onlinecourses.nptel.ac.in/noc20_ee76/preview

MR. CHANDRASINH DHIRUBHA PARMAR
Digitally signed by (Name of HOD)

DR. RAJENDRASINH BAHADURSINH JADEJA
Digitally signed by (Name of Dean/ Principal)