COURSE TITLE	**VLSI PHYSICAL DESIGN**
COURSE CODE	**01CT0717**
COURSE CREDITS	**4**

Objective:

1 The course will introduce the participants about basic design flow in VLSI physical design. This course will help students to understand the back-end design concepts.

Course Outcomes: After completion of this course, student will be able to:

1 Know the basic design flow in VLSI physical design domain
2 Understand the static timing analysis
3 Understand floor planning and partitioning
4 Analyze the clock routing
5 Know concepts of DFT and BIST
6 Analyze low power design techniques

Pre-requisite of course: Basic concepts in digital circuit design

Teaching and Examination Scheme

Theory Hours	Tutorial Hours	Practical Hours	ESE	IA	CSE	Viva	Term Work
3	0	2	50	30	20	25	25

Contents : Unit	Topics	Contact Hours
1	**Introduction** VLSI design styles, VLSI Physical Design flow	2
2	**Floor Planning and placement** Partitioning, floor planning and its algorithms, pin assignments,, placement,, classification of placement algorithms	4
3	**Routing** Grid routing, global routing, detail routing	4
4	**Clock design** Clock design issues, Clock distribution, clock skew and jitter, Clock network synthesis, set-up time and hold time, strategies to reduce clock skew, power and ground routing	8
5	**Timing analysis** Time closure, timing driven placement, Timing driven routing, static timing analysis,, slack calculation, timing analysis problems	6

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Contents : Unit	Topics	Contact Hours
6	**Physical Synthesis and interconnect** Physical synthesis, gate sizing, buffering, netlist restructuring, performance driven design flow. Timing optimization, interconnect modeling, wire geometry, layer stack, wire resistance, choice of metal, cross talk, Design rule check, Layout	6
7	**Design for Testability** Various sources of faults and types of faults, fault modeling, Design for testability, DFT techniques, scan path design, scan flip flop, boundary scan, built in self-test	6
8	**Low power design techniques** Types of power dissipation, Techniques to reduce power, gate level design for low power	6
Total Hours		**42**

Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
1	**Experiment-1** Explore the OpenROAD flow and develop the environment to use open source tools fot RTL2GDS flow	2
2	**Experiment-2** Perform RTL Synthesis of the design using yosys open synthesis tool.	2
3	**Experiment-3** Develop the data base using OpenDB for physical chip design.	2
4	**Experiment-4** Initialize the floor plan with necessary specifications.	2
5	**Experiment-5** Develop power grid planning using PDNGEN	2
6	**Experiment-6** Learn the pin placement using ioPlacer	2
7	**Experiment-7** Place an IO ring around the boundary of the a chip and connect with either wirebond pads or a bump array	2
8	**Experiment-8** Explore OpenSTA as a gate level static timing verifie anda as a stand-alone executable to verify the timing of a design using standard file formats	2
9	**Experiment-9** Perform the detailed placement analysis using OpenDP	2
10	**Experiment-10** Analyze clock tree synthesis using TritonCTS 2.0	2
11	**Experiment-11** Perform global routing using TritonRoute and do analysis of design.	2

Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
12	**Experiment-12** Do IR drop analysis using PDNSim	2
13	**Experiment-13** Perform parasitic extraction analysis using OpenRCX	2
14	**Experiment-14** Check antenna rules violations using Antenna Rule Checker and generate a report.	2
Total Hours		**28**

Textbook :

1 VLSI Physical Design Automation: Theory And Practice, Sait Sadiq M. Et.Al, Cambridge India, 2010

References:

1 VLSI Physical Design From Graph Partitioning to Timing Closure, VLSI Physical Design From Graph Partitioning to Timing Closure, Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu, Springer, 2012

Suggested Theory Distribution:

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery					
Remember / Knowledge	**Understand**	**Apply**	**Analyze**	**Evaluate**	**Higher order Thinking / Creative**
10.00	20.00	25.00	25.00	15.00	5.00

Instructional Method:

1 The internal evaluation will be done on the basis of continuous evaluation of students in the laboratory and class-room.

2 Practical examination will be conducted at the end of the semester for evaluation of performance of students in laboratory.

3 Students may use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory, etc.

4 The course delivery method will depend upon the requirement of content and need of the students. The teacher in addition to conventional teaching method (Chalk and Talk) may use any of the tools such as demonstration, role play, Quiz, brainstorming, Flipped class, Project based learning, Collaborative learning, MOOCs etc. for effective teaching.

Supplementary Resources:

1 https://nptel.ac.in/courses/106105161

Supplementary Resources:

2 https://www.youtube.com/watch?v=1rfBK5KKzR0

3 https://www.youtube.com/watch?v=OmEbzRp_NGg

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