COURSE TITLE	**FPGA BASED SYSTEM DESIGN**
COURSE CODE	**01CT0718**
COURSE CREDITS	**4**

Objective:

1 The main objective of this course is to provide the basics about internal architecture of FPGA and working of FPGA

Course Outcomes: After completion of this course, student will be able to:

1 Know the concepts of digital design
2 Understand evolution of programmable logic device
3 Learn FPGA architecture
4 Program the FPGA device
5 Develop FPGA based system

Pre-requisite of course: Digital circuit design

Teaching and Examination Scheme

Theory Hours	Tutorial Hours	Practical Hours	ESE	IA	CSE	Viva	Term Work
3	0	2	50	30	20	25	25

Contents : Unit	Topics	Contact Hours
1	**Revision of basic Digital systems.** Combinational Circuits, Sequential Circuits, Timing, Electrical Characteristics, Power Dissipation	4
2	**Current state of the field** SoC, IP Design, SoPC, Design methodology, System Modelling, Hardware- Software Co-design, Device Technology, Application Domains	6
3	**Digital system Design.** Top down Approach to Design, Case study, Data Path, Control Path, Controller behavior and Design, Case study Mealy & Moore Machines, Timing of sequential circuits, Pipelining, Resource sharing	6
4	**Programmable Logic Devices.** Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, Design Flow, Programmable Interconnections, Complex PLD's (MAX - 7000, APEX), Architecture, Resources, Applications, Tools	8

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Contents : Unit	Topics	Contact Hours
5	**FPGA Architecture** Introduction, Logic Block Architecture, Routing Architecture, Programmable Interconnections, Design Flow,Xilinx Virtex-II Architecture, Altera Stratix Architecture	6
6	**Programming the FPGA** Boundary Scan, Programming of the FPGA, Constraint Editor, Static Timing Analysis, One hot encoding, Applications, Tools, Case Study, Xilinx Virtex II Pro, Embedded System on Programmable Chip, Hardware-software co-simulation, Debugging FPGA Design	6
7	**HDL for Synthesis** Introduction, Behavioural, Data flow, Structural Models,Simulation Cycles, Process, Concurrent Statements, Sequential Statements,Loops, Delay Models, Sequential Circuits, FSM Coding	6
Total Hours		**42**

Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
1	**Experiment: 1** Introduction to the FPGA development board.	2
2	**Experiment: 2** Interfacing input/output devices on the FPGA development board.	2
3	**Experiment: 3** Implementing adder circuits such as half/full and ripple carry adder on the FPGA development board.	2
4	**Experiment: 4** Implement multiplexers and demultiplexers on the FPGA development board	2
5	**Experiment: 5** Implement encoders and decoders on the FPGA development board.	2
6	**Experiment: 6** 6. Implement code converters on the FPGA development board	2
7	**Experiment: 7** 7. Implement flip-flops and registers on the FPGA development board	2
8	**Experiment: 8** Implement a counter with a frequency divider on the FPGA development board.	2
9	**Experiment: 9** Implement Mealy and Moore machine examples on the FPGA development board.	2
10	**Experiment: 10** Implement a Traffic Light Controller on the FPGA development board.	2

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Suggested List of Experiments:

Contents : Unit	Topics	Contact Hours
11	**Experiment: 11** Implement Digital Alarm Clock on the FPGA development board.	2
12	**Experiment: 12** Implement 8 bit RISC processor on the FPGA development board.	2
13	**Experiment: 13** Implement FIR/IIR filter on the FPGA development board.	2
14	**Experiment: 14** Implement sensor-based systems on the FPGA development board.	2
15	**Experiment: 15** Implement vending machine on the FPGA development board.	2
Total Hours		**30**

Textbook :

1 Digital Design: Principles and Practices, Jon F Wakerly, Prentice Hall, 1990

References:

1 VHDL for programmable logic, VHDL for programmable logic, Kevin Skahil, Cypress, 1996

2 VHDL, analysis and modeling of digital systems, VHDL, analysis and modeling of digital systems, Zainalabedin Navabi, McGraw-Hill, 1997

3 Fundamentals of Digital Logic with Verilog Design, Fundamentals of Digital Logic with Verilog Design, Stephen Brown, McGraw-Hill, 2002

4 Digital VLSI Systems Design: A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog, Digital VLSI Systems Design: A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog, Seetharaman Ramachandran, Springer, 2007

Suggested Theory Distribution:

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

Distribution of Theory for course delivery					
Remember / Knowledge	**Understand**	**Apply**	**Analyze**	**Evaluate**	**Higher order Thinking / Creative**
15.00	15.00	40.00	10.00	10.00	10.00

Instructional Method:

1 The internal evaluation will be done on the basis of continuous evaluation of students in the laboratory and class-room.

2 Practical examination will be conducted at the end of the semester for evaluation of performance of students in laboratory.

MR. CHANDRASINH DHIRUBHA PARMAR
Digitally signed by (Name of HOD)

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Instructional Method:

3 Students may use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory, etc.

4 The course delivery method will depend upon the requirement of content and need of the students. The teacher in addition to conventional teaching method (Chalk and Talk) may use any of the tools such as demonstration, role play, Quiz, brainstorming, Flipped class, Project based learning, Collaborative learning, MOOCs etc. for effective teaching.

Supplementary Resources:

1 https://nptel.ac.in/courses/117108040

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