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|---|---|
| **COURSE TITLE** | **INTRODUCTION TO HDL** |
| **COURSE CODE** | **01CT1551** |
| **COURSE CREDITS** | **3** |

**Objective:**

1 Introduce learners with Verilog/VHDL. Make students learn designing of digital circuits using behavioral and RTL modeling styles. Give exposure to learners to verify designed models, synthesizing them for target FPGA or using standard cell libraries.

**Course Outcomes:** After completion of this course, student will be able to:

1 Understand and use the architectural features available on the advance programmable hardware like FPGA and CPLD.

2 Apply the constructs of the HDL language to implement the functionality in hardware.

3 Analyze the given HDL code and infer the RTL design.

4 Evaluate the functionality of the designed modules by writing effective testbench.

5 Design digital components and circuits that are testable, reusable and synthesizable

**Pre-requisite of course:**Digital electronics, Basic Electronic

**Teaching and Examination Scheme**

| Theory Hours | Tutorial Hours | Practical Hours | ESE | IA | CSE | Viva | Term Work |
|---|---|---|---|---|---|---|---|
| 3 | 0 | 0 | 50 | 30 | 20 | 0 | 0 |

| Contents : Unit | Topics | Contact Hours |
|---|---|---|
| 1 | **Module 1: Introduction to Hardware Description Language (HDL):** Logic Elements, Expressions, Modules and Ports, Built-in Primitives, User-Defined Primitives, Dataflow Modeling, Behavioral Modeling, Structural Modeling, Task & Functions | 6 |
| 2 | **Module 2: Combinational Logic Design** Gates, Adders, Subtractor, Multiplexer, Decoder, Fast adders' structure (like look ahead carry adder, Carry Skip Adder etc.), Multiplier Architectures (like Serial multiplier, Parallel Multiplier etc.) | 6 |
| 3 | **Module 3: Sequential Logic Design** Flip-Flops, Counters, Synchronous and Asynchronous Sequential Machine, Pulse Mode Asynchronous Sequential Machines | 10 |
| 4 | **Module 4: Computer Arithmetic Design** Fixed Point Addition, Subtraction, Multiplication, Division; ALU; Decimal Addition, Subtraction, Multiplication, Division, Floating Point Addition, Subtraction, Multiplication, Division | 8 |

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| Contents : Unit | Topics | Contact Hours |
|---|---|---|
| 5 | **Module 5: CPU Modeling**<br>Computer Model – CPU model specification, designing CPU,, Designing of Datapath, Designing of Control Path, HDL Description – CPU Datapath, Control Path and Top Module, CPU Testing – Testbench to verify the functionality | 8 |
| 6 | **Module 6: Programmable Hardware Architectures**<br>Architecture and applications of Read Only Memory (ROM), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Field Programmable Gate Array (FPGA), Complex Programmable Logic Design (CPLD) | 4 |
| **Total Hours** | | **42** |

**Textbook :**


1 Verilog HDL Design Examples, Joseph Cavanagh, CRC Press, 2017

2 Verilog HDL A Guide to Digital Design and Synthesis · Volume 1, Samir Palnitkar, SunSoft Press, 2003

3 Verilog Digital System Design, Zainalabedin Navabi, McGraw Hill LLC, 2006

4 Circuit Design with VHDL, Volnei A. Pedroni, MIT Press, 2020

5 VHDL Programming by Example, Douglas L. Perry, McGraw Hill LLC, 2002


**References:**


1 IEEE Standard for Verilog Hardware Description Language. New York: IEEE, IEEE Standard for Verilog Hardware Description Language. New York: IEEE, IEEE, IEEE, 2005


**Suggested Theory Distribution:**

The suggested theory distribution as per Bloom's taxonomy is as follows. This distribution serves as guidelines for teachers and students to achieve effective teaching-learning process

| Distribution of Theory for course delivery | | | | | |
|---|---|---|---|---|---|
| **Remember / Knowledge** | **Understand** | **Apply** | **Analyze** | **Evaluate** | **Higher order Thinking / Creative** |
| 10.00 | 15.00 | 30.00 | 20.00 | 10.00 | 15.00 |

**Instructional Method:**

1 The course delivery method will depend upon the requirement of the content and need of the students. The teacher in addition to the conventional teaching method (Chalk and Talk) may use any of the tools such as demonstration, role play, Quiz, brainstorming, MOOCs etc. for effective teaching.

2 The internal evaluation will be done on the basis of continuous evaluation of students in the class-room

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**Instructional Method:**

3 Students may use supplementary resources such as online videos, NPTEL videos, e-courses, Virtual Laboratory, etc.

**Supplementary Resources:**

1 https://www.youtube.com/playlist?list=PLUtfVcb-iqn-EkuBs3arreilxa2UKIChl

2 https://www.electronicsforu.com/electronics-projects/microprocessor-data-path-nexys- 4-ddr

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